REMARKS

The Applicants respectfully request reconsideration and allowance of Claims 1-18 in view of the following arguments.

INTERVIEW SUMMARY

The Applicants appreciate the telephone interview conducted on April 20, 2005, between Examiner Tat and the undersigned attorney. In the interview, the undersigned attorney summarized the arguments presented below, in particular, emphasizing the fundamental distinctions between the logic circuit design disclosed in Yee et al., "Dynamic Logic Synthesis," IEEE, 1997, pp. 345-348 ("Yee") and the logic circuit design required in the present claims. No agreement was reached as to the allowability of the claims.

STATUS OF THE CLAIMS

The present application was filed with claims 1-18. Claims 1, 8, and 13 are independent claims, while claims 2 through 7, 9 through 12, and 14 through 18 are dependent. None of the claims have been amended.

CLAIMS 1-18 ARE NOT ANTICIPATED BY THE CITED PRIOR ART

The Examiner rejected claims 1 through 18 under 35 U.S.C. § 102(b) as being anticipated by Yee et al. ("Dynamic Logic Synthesis," IEEE, 1997, pp 345-348, hereinafter referred to as "Yee"). The Applicants respectfully submit that the claims are not anticipated by Yee.

Claim 1 requires the following elements:

A method of designing a logic circuit to provide a predetermined logical operation, the method including the steps of:

(a) defining a logic synthesis block comprising a dynamic logic circuit;

(b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit, the logic synthesis being performed utilizing a synthesis library constrained to the logic synthesis block;

(c) eliminating unused devices in the intermediate circuit to produce a final circuit; and

(d) sizing the devices in the final circuit.

In the Office Action, the Examiner appears to be equating the "circuit netlist" in Figure 7 of Yee with the "intermediate circuit" of Applicants' claim 1. Yee fails to disclose eliminating unused devices in the circuit netlist ("intermediate circuit") to produce a final circuit as required in Applicants' independent claim 1. In fact, once this circuit netlist is generated, rather than eliminating unused devices from the netlist, delay elements are added to the netlist (see Yee, page 347, col. 1, Fig. 7 description). Further, Yee fails to address utilizing a synthesis library constrained to a logic synthesis block as required in claim 1. Neither the "cell and delay library" nor the "library characterization," both of Figure 7 in Yee, appears to be constrained to a logic synthesis block as required for the logic circuit design method of Applicants' claim 1. In addition to the requirements of claim 1, Applicants' specification includes a definition of the logic synthesis step being "constrained" to a circuit library including only the logic synthesis block (see Figure 4 and its accompanying description). Specifically, in Figure 4, each logic synthesis block 33 to 33i, 34 to 34i, 35 to 35i, or 36 to 36i in each string 30 to 30i comprises the circuit defined as the logic synthesis block for purposes of performing logic synthesis. Also, although Yee illustrates in Figure 7 that logic synthesis is part of a design methodology, Yee fails to show "defining a logic synthesis block comprising a dynamic logic circuit" as required by each of Applicants' independent claims 1, 8, and 13.

For all of these reasons, Applicants urge the Examiner to withdraw the § 102(b) rejection of independent claims 1, 8, and 13 as being anticipated by Yee.

The Examiner refers to Figure 8 of Yee as showing the step of defining the logic synthesis block as required in claims 2, 9, and 15. However, Yee does not disclose defining a logic synthesis block at all. Thus, Applicants respectfully submit that claims 2, 9, and 15 are not only allowable as being dependent upon an allowable claim, but also in view of requirements that this directly adds.

Regarding dependent claims 3, 10, and 16, as stated above, Yee fails to show a logic synthesis block at all and certainly does not show a logic synthesis block comprising a four high and four wide dynamic AND/OR circuit. Thus, Applicants urge the Examiner to withdraw the § 102(b) rejection of dependent claims 3, 10, and 16 as being dependent upon an allowable claim and in view of the limitation they directly add.

Regarding dependent claims 4, 11, and 17, Yee fails to disclose performing logic synthesis that includes leaving the size of devices in a logic synthesis block substantially unconstrained. Because Yee does not disclose a logic synthesis block, Yee also cannot disclose leaving the size of devices in a logic synthesis block substantially unconstrained. For these reasons, Applicants respectfully request the Examiner to withdraw the § 102(b) rejection of dependent claims 4, 11, and 17.

Regarding dependent claim 5, as stated with regard to independent claim 1, Yee discloses adding delay elements to the circuit netlist. Yee fails to eliminate unused devices from an intermediate circuit. Yee also fails to disclose detecting devices that have a constant state as the

intermediate circuit operates to provide predetermined logical operations.. For all of these reasons, Applicants urge the Examiner to withdraw the § 102(b) rejection of dependent claim 5.

Regarding dependent claim 6, Yee fails to disclose analyzing a final circuit to determine characteristics of each device in the final circuit necessary in order to consistently provide the predetermined logical operation and meet drive requirements. Thus, Applicants believe dependent claim 6 is allowable as being dependent upon an allowable claim and in view of the limitation that it directly adds..

Regarding dependent claims 7, 12, and 18, as stated above, Yee fails to disclose defining a logic synthesis block at all, thus, Yee must fail to disclose a logic synthesis block reset signal. For all of these reasons, Applicants urge the Examiner to withdraw the § 102(b) rejection of dependent claims 7, 12, and 18.

CONCLUSION

For all of the above reasons, the Applicants respectfully request reconsideration and allowance of claims 1-18.

If any issue remains as to the allowability of these claims, or if a conference might expedite allowance of the claims, the Examiner is asked to telephone the undersigned attorney prior to issuing a further action in this case.

Respectfully submitted,

THE CULBERTSON GROUP

Dated: 3 May 2005

By: Russell C. Scott

Russell D. Culbertson, Reg. No. 32,124
Russell C. Scott, Reg. No. 43,103
Trevor Lind, Reg. No. 54,785
1114 Lost Creek Blvd.
Suite 420
Austin, Texas 78746
512-327-8932
ATTORNEYS FOR APPLICANTS

CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, (Fax No. 703-872-9306) on May 3, 2005.

Russell C. Scott, Reg. No. 43,103 Russell C. Scott

161.ROA.3-29-05.rev2.wpd